

MAR 04 2004

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| To: Commissioner for Patents for Examiner Unknown Group Art Unit 2816 | Facsimile No.: 703/872-9306 |
| From: Kit Cruz-Verona for Krista Douthitt Paralegal to Duke Yee | No. of Pages Including Cover Sheet: 6 |
| Message: Enclosed herewith: <ul style="list-style-type: none">• Transmittal Document; and• Preliminary Amendment. | |
| Re: Application No. 10/696,139 Attorney Docket No: YOR920030387US1 | |
| Date: Thursday, March 4, 2004 | |
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rhee et al.

Serial No.: 10/696,139

Filed: October 29, 2003

For: Semidigital Delay-Locked Loop
Using an Analog-Based Finite State
Machine§
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Group Art Unit: 2816

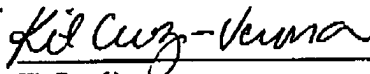
Examiner: Unknown

Attorney Docket No.: YOR920030387US1

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By:


Kit Cruz-VeronaTRANSMITTAL DOCUMENTCommissioner for Patents
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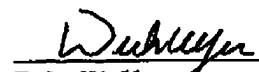
Sir:

ENCLOSED HEREWITH:

- Preliminary amendment.

No fees are believed to be necessary. If, however, any fees are required, I authorize the Commissioner to charge these fees to Deposit Account No. 50-0510. No extension of time is believed to be necessary. If, however, an extension of time is necessary, I authorize the Commissioner to charge the necessary extension fees to Deposit Account No. 50-0510.

Respectfully submitted,


Duke W. Yee
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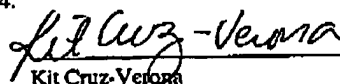
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By:


Kit Cruz-VeronaPRELIMINARY AMENDMENTCommissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

No fees are believed to be necessary. If, however, any fees are required, I authorize the Commissioner to charge these fees to Deposit Account No. 50-0510. No extension of time is believed to be necessary. If, however, an extension of time is necessary, I authorize the Commissioner to charge the necessary extension fees to Deposit Account No. 50-0510.

Prior to continued examination of this application, please amend the above-identified application as follows:

IN THE CLAIMS

1. (Original) A semidigital delay-locked loop circuit comprising:

a controllable delay element having a clock input and a phase input, and a clock signal output, wherein signals on the clock signal output have a changing phase controlled by phase data received at the phase input;

a phase detector, a first input, a second input, an up output, a down output, and a data output, wherein data is received at the first input, the second input is connected to the clock signal output, and